UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,863	12/08/2006	Nigel Peter Smith	427008026US	7198

34036 7590 12/23/2008

Silicon Valley Patent Group LLP
18805 Cox Avenue
Suite 220
Saratoga, CA 95070

EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
12/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/549,863	SMITH ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

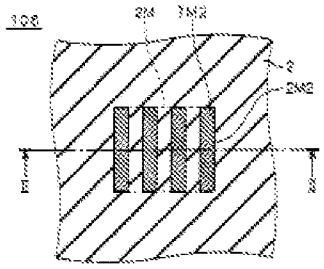
Claim Rejections - 35 USC § 102

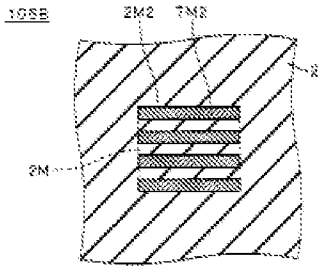
1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

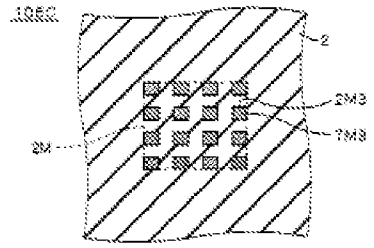
> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 35 l(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21 (2) of such treaty in the English language.

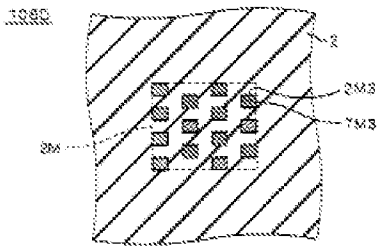
2. Claims 1-6, 8-21 and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujiki et al., U.S. Patent 6,677,682 B1.

Fujiki teaches an overlay metrology mark as claimed. See FIGS. **1-21**, where Fujiki teaches the following limitations.









Pertaining to claim 1, Fujiki teaches an overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with a first layer and a second mark portion associated with a second layer, wherein each mark portion comprises a single two dimensional generally orthogonal array of individual test structures.

Pertaining to claim 2, Fujiki teaches an overlay metrology mark in accordance with claim 1 wherein each mark portion is developed within or on the said layer.

Pertaining to claim 3, Fujiki teaches an overlay metrology mark in accordance with claim 2 wherein each mark portion is printed on the said layer by a microlithographic process.

Pertaining to claim 4, Fujiki teaches an overlay metrology mark in accordance with any preceding claim wherein each mark portion comprises a single two dimensional generally substantially square array of individual test structures with generally constant spacing between test structures throughout the array.

Pertaining to claim 5, Fujiki teaches an overlay metrology mark in accordance with any preceding claim wherein the spacing between test structures in the array comprising the first mark portion and the spacing between the test structures in the array comprising the second mark portion is equivalent (please note that because Fujiki disclose diffraction patterns, it would be necessary to have equivalent spacing's).

Pertaining to claim 6, Fujiki teaches an overlay metrology mark in accordance with any preceding claim wherein each mark portion has a generally square overall outline.

Pertaining to claim 8, Fujiki teaches an overlay metrology mark in accordance with any preceding claim wherein spacing between test structures in the array is between one and four structure widths.

Pertaining to claim 9, Fujiki teaches an overlay metrology mark in accordance with any preceding claim wherein the individual test structures making up each array are substantially identically sized and shaped and have generally square geometry.

Pertaining to claim 10, Fujiki teaches an overlay metrology mark in accordance with any preceding claim wherein the individual test structures comprise arrangement of design rule sized sub-structures.

Pertaining to claim 11, Fujiki teaches an overlay metrology mark in accordance with claim 10 wherein the arrangements of design rule sized sub-structures are selected from parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array, arrays of holes within a suitably shaped test structure and any combinations of these or other like patterns.

Pertaining to claim 12, Fujiki teaches an overlay metrology mark in accordance with claim 10 or 11 wherein sub-structures are of design rule dimensions.

Pertaining to claim 13, Fujiki teaches an overlay metrology mark in accordance with any preceding claim wherein the arrays of test structures making up the first and second mark portions are disposed such that the first portion overlays the second portion and that the test structures of second portion are arrayed within the gaps between the test structures of the first portion and visible therebetween.

Pertaining to claim 14, Fujiki teaches an overlay metrology mark in accordance with claim 13

wherein each test structure in the second portion is located at the diagonal center of a square bounded at each comer by test structures of the first portion.

Pertaining to claim 15, Fujiki teaches an overlay metrology mark in accordance with any one of claims 1 to 12 wherein the test structures making up the first and second mark portions are disposed such that the first portion is laterally spaced from the second portion in a spacing direction parallel to a horizontal or vertical direction of the square arrays such that a notional line in the spacing direction can be drawn about which each array exhibits mirror symmetry.

Pertaining to claim 16, Fujiki teaches an overlay metrology mark in accordance with claim 15 wherein each mark portion comprises an identical pattern of test structures.

Pertaining to claim 17, Fujiki teaches a method for providing an overlay metrology mark to determine the relative position between two or more layers of an integrated circuit structure comprises the steps of: laying down a first mark portion in association with a first layer; and laying down a second mark portion in association with a second layer; wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures.

Pertaining to claim 18, Fujiki teaches a method for determining the relative position between two or more layers of an integrated circuit structure comprises the steps of: laying down a first mark

portion in association with a first layer r; laying down a second mark portion in association with a second layer; wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures optically imaging the two mark portions; collecting and digitizing the image; numerically analysing the digitized data to obtain a quantified measurement of the misalignment of the first and second mark portions.

Pertaining to claim 19, Fujiki teaches the method of claim 18 wherein optical imaging of the mark is carried out using bright field microscopy.

Pertaining to claim 20, Fujiki teaches the method of one of claims 17 to 19 wherein each mark portion is developed within or on the said layer.

Pertaining to claim 21, Fujiki teaches the method of one of claims 17-20 wherein each mark portion is laid down by a microlithographic process.

Pertaining to claim 23, Fujiki teaches the method of claim 18 wherein individual mark portions are developed within or on the layer.

Pertaining to claim 24, Fujiki teaches the method of claim 18 wherein individual mark portions are formed by a microlithographic process.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiki et al., U.S. Patent 6,420,791 B 1.

Fujiki fails to disclose the width of the test structure. However, it is well known in the art that the alignment mark size is critical of the feature size for the device in question, i.e., large device, large feature size, large alignment mark. One of the reasons that the alignment mark is near the feature size of the device is to maintain real estate symmetry. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation.

Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the

difference is really unexpected. In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)

Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. Exparte Ishizaka, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175,201 USPQ 67 (CCPA 1979).

Please note that claims 23 and 24 were inadvertently missed during the examination mailed May 28, 2008.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W. David Coleman/
Primary Examiner, Art Unit 2823